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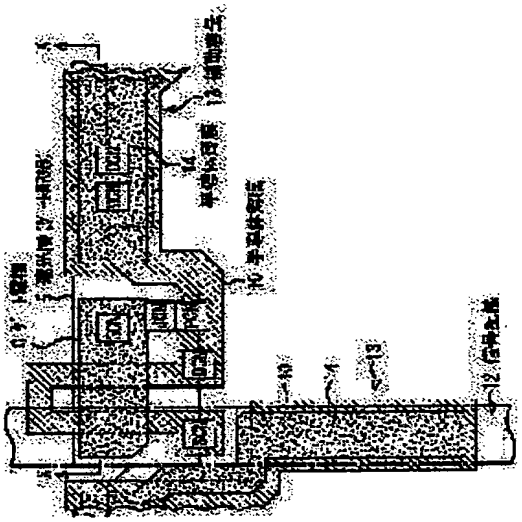
(54) THIN-FILM SEMICONDUCTOR DEVICE, LIQUID CRYSTAL DISPLAY, AND MANUFACTURING METHODS FOR THEM

(57)Abstract:
PROBLEM TO BE SOLVED: To improve the pixel aperture rate of a thin-film semiconductor device used as a drive substrate of an active matrix liquid crystal display.
SOLUTION: The thin-film semiconductor device has a plurality of signal wirings 12 and a mutually intersected gate wiring, and a pixel is arranged at each intersection of both wirings on an insulating substrate. Each pixel contains at least a pixel electrode, a thin-film transistor for driving the pixel electrode, and a light shading belt 5 for shielding a thin-film transistor from the external light. The source of the thin film transistor is connected with the signal wiring 12, and a drain is connected with the pixel electrode. A gate electrode (G) is connected with the gate wiring. The light shading belt 5 consists of the first conductive layer and at least a part of the shading belt 5 is used to the gate wiring. The gate electrode (G) consists of a second conductive layer which is different from the first conductive layer. The first conductive layer used as the gate wire and the second conductive layer as the gate electrode G are connected mutually in each pixel electrically via a contact hole GCN.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] It has two or more signal wiring and gate wiring which cross mutually, and the pixel allotted to each intersection of both wiring on an insulating substrate. Each pixel The protection-from-light band which covers at least a pixel electrode, the thin film transistor which drives this, and this thin film transistor from outdoor daylight is included. In the thin film semiconductor equipment by which the source of this thin film transistor is connected to this signal wiring, a drain is connected to this pixel electrode, and the gate electrode is connected to this gate wiring said protection-from-light band It consists of the first conductive layer and at least a part is used for this gate wiring. Said gate electrode Thin film semiconductor equipment with which this first conductive layer that consists of the second different conductive layer from the first conductive layer, and is used for gate wiring, and this second conductive layer that becomes a gate electrode are characterized by connecting electrically mutually within each pixel.
[Claim 2] The part of each second conductive layer which the second conductive layer which constitutes said gate electrode is divided for every pixel, and was divided is thin film semiconductor equipment according to claim 1 characterized by connecting with this first conductive layer used for this gate wiring within each pixel electrically.
[Claim 3] The part of each first conductive layer which the first conductive layer which constitutes said gate wiring is divided for every pixel, and was divided is thin film semiconductor equipment according to claim 1 characterized by connecting with this second conductive layer that serves as this gate electrode within each pixel electrically.
[Claim 4] Said protection-from-light band is thin film semiconductor equipment according to claim 1 characterized by consisting of a conductive layer of the bilayer which covers this thin film transistor from up-and-down [both], and using the one of the two for this gate wiring as the first conductive layer.
[Claim 5] Said protection-from-light band is thin film semiconductor equipment according to claim 1 characterized by consisting of a conductive layer of the monolayer which covers this thin film transistor from up-and-down inner one side, and using this for this gate wiring as the first conductive layer.
[Claim 6] Each pixel is thin film semiconductor equipment according to claim 1 characterized by being the second conductive layer and this layer from which one side of the electrode of this vertical pair constitutes this gate electrode including the auxiliary capacity which sandwiched the dielectric with the electrode of a vertical pair in order to hold the signal charge written in this pixel electrode from signal wiring through this thin film transistor.
[Claim 7] It consists of a substrate of the pair mutually joined through the predetermined gap, and liquid crystal held in this gap. One substrate While it has the pixel allotted to each intersection of two or more signal wiring and gate wiring which cross mutually, and both wiring, the substrate of another side has the electrode which counters each pixel. Each pixel The protection-from-light band which covers at least a pixel electrode, the thin film transistor which drives this, and this thin film transistor from outdoor daylight is included. In the liquid crystal display by which the source of this thin film transistor is

connected to this signal wiring, a drain is connected to this pixel electrode, and the gate electrode is connected to this gate wiring said protection-from-light band It consists of the first conductive layer and at least a part is used for this gate wiring. Said gate electrode The liquid crystal display with which this first conductive layer that consists of the second different conductive layer from the first conductive layer, and is used for gate wiring, and this second conductive layer that becomes a gate electrode are characterized by connecting electrically mutually within each pixel.

[Claim 8] The part of each second conductive layer which the second conductive layer which constitutes said gate electrode is divided for every pixel, and was divided is a liquid crystal display according to claim 7 characterized by connecting with this first conductive layer used for this gate wiring within each pixel electrically.

[Claim 9] The part of each first conductive layer which the first conductive layer which constitutes said gate wiring is divided for every pixel, and was divided is a liquid crystal display according to claim 7 characterized by connecting with this second conductive layer that serves as this gate electrode within each pixel electrically.

[Claim 10] Said protection-from-light band is a liquid crystal display according to claim 7 characterized by consisting of a conductive layer of the bilayer which covers this thin film transistor from up-and-down [both], and using the one of the two for this gate wiring as the first conductive layer.

[Claim 11] Said protection-from-light band is a liquid crystal display according to claim 7 characterized by consisting of a conductive layer of the monolayer which covers this thin film transistor from up-and-down inner one side, and using this for this gate wiring as the first conductive layer.

[Claim 12] Each pixel is a liquid crystal display according to claim 7 characterized by being the second conductive layer and this layer from which one side of the electrode of this vertical pair constitutes this gate electrode including the auxiliary capacity which sandwiched the dielectric with the electrode of a vertical pair in order to hold the signal charge written in this pixel electrode from this signal wiring through this thin film transistor.

[Claim 13] It has two or more signal wiring and gate wiring which cross mutually, and the pixel allotted to each intersection of both wiring on an insulating substrate. Each pixel The protection-from-light band which covers at least a pixel electrode, the thin film transistor which drives this, and this thin film transistor from outdoor daylight is included. In the manufacture approach of thin film semiconductor equipment that the source of this thin film transistor is connected to this signal wiring, a drain is connected to this pixel electrode, and the gate electrode is connected to this gate wiring Said protection-from-light band uses the part for this gate wiring at least while forming it by the first conductive layer. Said gate electrode The manufacture approach of the thin film semiconductor equipment characterized by connecting mutually electrically this second conductive layer that becomes this first conductive layer that forms by the second different conductive layer from the first conductive layer, and is used for gate wiring, and a gate electrode within each pixel.

[Claim 14] The manufacture approach of the thin film semiconductor equipment according to claim 13 characterized by connecting with this first conductive layer that uses the part of each second divided conductive layer for this gate wiring within each pixel electrically while dividing the second conductive layer which constitutes said gate electrode for every pixel.

[Claim 15] The manufacture approach of the thin film semiconductor equipment according to claim 13 characterized by connecting the part of each first divided conductive layer with this second conductive layer that serves as this gate electrode within each pixel electrically while dividing the first conductive layer which constitutes said gate wiring for every pixel.

[Claim 16] Said protection-from-light band is the manufacture approach of the thin film semiconductor equipment according to claim 13 characterized by forming by the conductive layer of the bilayer which covers this thin film transistor from up-and-down [both], and using the one of the two for this gate wiring as the first conductive layer.

[Claim 17] Said protection-from-light band is the manufacture approach of the thin film semiconductor equipment according to claim 13 characterized by forming by the conductive layer of the monolayer which covers this thin film transistor from up-and-down inner one side, and using this for this gate

wiring as the first conductive layer.

[Claim 18] The manufacture approach of the thin film semiconductor equipment according to claim 13 characterized by forming in each pixel the auxiliary capacity which sandwiched the dielectric with the electrode of a vertical pair in order to hold the signal charge written in this pixel electrode through this thin film transistor from this signal wiring, and forming so that it may become the second conductive layer and this layer from which one side of the electrode of this vertical pair constitutes this gate electrode.

[Claim 19] It consists of a substrate of the pair mutually joined through the predetermined gap, and liquid crystal held in this gap. While forming the pixel allotted to each intersection of two or more signal wiring and gate wiring which intersect one substrate mutually, and both wiring, the electrode which counters each pixel is formed in the substrate of another side. To each pixel The protection-from-light band which covers at least a pixel electrode, the thin film transistor which drives this, and this thin film transistor from outdoor daylight is formed. In the manufacture approach of the liquid crystal display which connects the source of this thin film transistor to this signal wiring, connects a drain to this pixel electrode, and connects a gate electrode to this gate wiring said protection-from-light band While forming by the first conductive layer, the part is used for this gate wiring at least. Said gate electrode The manufacture approach of the liquid crystal display characterized by connecting mutually electrically this second conductive layer that becomes this first conductive layer that forms by the second different conductive layer from the first conductive layer, and is used for gate wiring, and a gate electrode within each pixel.

[Claim 20] The manufacture approach of the liquid crystal display according to claim 19 characterized by connecting with this first conductive layer that uses the part of each second divided conductive layer for this gate wiring within each pixel electrically while dividing the second conductive layer which constitutes said gate electrode for every pixel.

[Claim 21] The manufacture approach of the liquid crystal display according to claim 19 characterized by connecting the part of each first divided conductive layer with this second conductive layer that serves as this gate electrode within each pixel electrically while dividing the first conductive layer which constitutes said gate wiring for every pixel.

[Claim 22] Said protection-from-light band is the manufacture approach of the liquid crystal display according to claim 19 characterized by forming by the conductive layer of the bilayer which covers this thin film transistor from up-and-down [both], and using the one of the two for this gate wiring as the first conductive layer.

[Claim 23] Said protection-from-light band is the manufacture approach of the liquid crystal display according to claim 19 characterized by forming by the conductive layer of the monolayer which covers this thin film transistor from up-and-down inner one side, and using this for this gate wiring as the first conductive layer.

[Claim 24] The manufacture approach of the liquid crystal display according to claim 19 characterized by forming in each pixel the auxiliary capacity which sandwiched the dielectric with the electrode of a vertical pair in order to hold the signal charge written in this pixel electrode through this thin film transistor from this signal wiring, and forming so that it may become the second conductive layer and this layer from which one side of the electrode of this vertical pair constitutes this gate electrode.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to thin film semiconductor equipment and liquid crystal displays, and these manufacture approaches. It is related with thin film semiconductor equipment in more detail at the gate wiring structure and protection-from-light structure of a thin film transistor by which accumulation formation is carried out.
[0002]
[Description of the Prior Art] The thin film semiconductor equipment which carried out accumulation formation of a thin film transistor or the pixel electrode is used abundantly at the drive substrate of a liquid crystal display. In order to cover a thin film transistor from a strong light source light of a projector, protection-from-light structure has become indispensable, and especially the thin film semiconductor equipment built into the liquid crystal display for projectors shows the example to drawing 5 . Since the pixel electrode 8 is driven, the liquid crystal display uses the thin film transistor, so that it may illustrate. Although this thin film transistor is for example, elevated-temperature poly-Si TFT, it is also possible to replace with this and to use low-temperature poly-Si TFT and amorphous silicon TFT. The liquid crystal display of illustration is indicated by JP,2000-131716,A. This liquid crystal display is equipped with the substrate 1 (it consists of a quartz which supports TFT) which has TFT7 which is a pixel transistor, and the opposite substrate 2, and liquid crystal 3 is held between a substrate 1 and the opposite substrate 2 so that it may illustrate. The opposite substrate 2 is equipped with the counterelectrode 6.
[0003] A substrate 1 has the pixel electrode 8 in a management, and has TFT(here thin film transistor, TFT of top gate structure) 7 in the lower layer section. TFT7 plays a role of a switching element which drives the pixel electrode 8. TFT7 makes the barrier layer the semi-conductor thin film 10 which consists of polycrystalline silicon. This semi-conductor thin film 10 consists of first pass polish recons (1poly). the semi-conductor thin film 10 top -- SiO2 etc. -- from -- the gate electrode G is formed through the becoming gate dielectric film 11. This gate electrode G consists of second layer polish recons (2poly). TFT7 has the source field S and the drain field D on both sides of the gate electrode G. The LDD field is formed in the source / drain edge. The drawer electrodes 12A and 12B have connected with the source field S and the drain field D respectively. Each drawer electrodes 12A and 12B can be formed with aluminum system ingredients, such as aluminum. Electrical connection of the drawer electrode 12A is carried out to the source field S of TFT7 through a contact hole SCN, and, similarly electrical connection of the drawer electrode 12B of another side is carried out to the drain field D of TFT7 through the contact hole DCN.
[0004] The auxiliary capacity 13 (Cs) is formed in the semi-conductor thin film 10. SiO2 which this auxiliary capacity 13 (Cs) is with the first pass polish recon (1poly) which constitutes the semi-conductor thin film 10 7, i.e., TFT, and the second layer polish recon (2poly) which constitutes the semi-conductor thin film 14 G, i.e., a gate electrode, and constitutes gate dielectric film 11 etc. -- a dielectric film is inserted.

[0005] The protection-from-light layers 4M and 4P are formed in the medium-rise section between the management which has the pixel electrode 8, and the lower layer section in which TFT7 is formed. This is a protection-from-light layer which is in the opposite substrate 2, i.e., incidence, side to TFT7, and is called the "upper protection-from-light layer." The upper protection-from-light layer consists of mask protection-from-light layer 4M and pad protection-from-light layer 4P. To the incident light from the opposite substrate 2 side, it pulled out with the two upper protection-from-light layers (mask protection-from-light layer 4M and Bud protection-from-light layer 4P), and protection from light of all fields other than pixel opening is accomplished by the superposition of Electrodes 12A and 12B (here, it forms by aluminum). Both mask protection-from-light layer 4M and pad protection-from-light layer 4P consist of metal membranes, such as the ingredient which has conductivity, for example, Ti etc. Along with the line writing direction (longitudinal direction) of a pixel, patterning of mask protection-from-light layer 4M is carried out continuously, and they shade TFT partially at least. Patterning of pad protection-from-

-from-

contact hole PCN. Pad protection-from-light layer 4P are pulled out through a contact hole JCN, and are connected to electrode 12B. It pulls out to the appearance mentioned above and electrical connection of the electrode 12B is carried out to the drain field D of TFT7 through the contact hole DCN. All fields other than pixel opening are shaded by mask protection-from-light layer 4M and pad protection-from-light layer 4P, and the superposition of the drawer electrodes 12A and 12B to the incidence from an opposite substrate side.

[0006] On the other hand, the protection-from-light layer 5 is formed in the reverse side in the opposite substrate 2 of the pixel transistor section. This is called a "lower layer protection-from-light layer." The source / drain edge of the pixel transistor 7 at least are shaded in this lower layer protection-from-light layer 5. Thus, the LDD fields 71 and 72 are formed in the source / drain edge currently shaded. Generally the lower layer protection-from-light layer 5 is formed from the silicide of a refractory metal. For example, it consists of WSi and has the thickness of 200nm.

[0007]

[Problem(s) to be Solved by the Invention] Corresponding to the raise in the brightness of the liquid crystal projector to accelerate, the improvement in permeability of a liquid crystal panel as shown in _____ is demanded in recent years. It doubles and maintenance of the image grace under the large quantity of light emitted from the light source for projectors is demanded. Conventionally, maintenance of the permeability improvement by the improvement in (1) pixel numerical aperture and the image grace by the increase of (2) auxiliary capacity (Cs area) is carried out as technique for it, and it has replied to the demand of a commercial scene. However, technique (1) and (2) essentially conflict. That is, increase of Cs area is directly linked with decline in a numerical aperture as it is. Conventionally, it could be parallel, and the technique of of (1) and (2) was able to be advanced because there were pixel layout top allowances. However, highly minute-ization of a liquid crystal projector takes for progressing, and the allowances on a layout are already impossible on the production of the conventional pixel structure, in order to be lost and to attain much more high numerical aperture-

[0008] _____ is the typical top view of the conventional liquid crystal display shown in _____ , and expresses only 1 pixel. The liquid crystal display is equipped with two or more signal wiring 12 and gate wiring which cross mutually so that it may illustrate. The pixel is prepared in the intersection with gate wiring arranged on the signal wiring 12 allotted in the direction of a train (lengthwise direction), and a line writing direction (longitudinal direction). A pixel contains a pixel electrode, the thin film transistor which drives this, and the protection-from-light band (protection-from-light layer) which covers a thin film transistor from outdoor daylight. The thin film transistor makes the semi-conductor thin film 10 the barrier layer, it connected with signal wiring 12 through the contact hole SCN, and,

formed with the semi-conductor thin film (2poly) which becomes layer with the another semi-conductor

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[0005] The protection-from-light layers 4M and 4P are formed in the medium-rise section between the management which has the pixel electrode 8, and the lower layer section in which TFT7 is formed. This is a protection-from-light layer which is in the opposite substrate 2, i.e., incidence, side to TFT7, and is called the "upper protection-from-light layer." The upper protection-from-light layer consists of mask protection-from-light layer 4M and pad protection-from-light layer 4P. To the incident light from the opposite substrate 2 side, it pulled out with the two upper protection-from-light layers (mask protection-from-light layer 4M and Bud protection-from-light layer 4P), and protection from light of all fields other than pixel opening is accomplished by the superposition of Electrodes 12A and 12B (here, it forms by aluminum). Both mask protection-from-light layer 4M and pad protection-from-light layer 4P consist of metal membranes, such as the ingredient which has conductivity, for example, Ti etc. Along with the line writing direction (longitudinal direction) of a pixel, patterning of mask protection-from-light layer 4M is carried out continuously, and they shade TFT partially at least. Patterning of pad protection-from-light layer 4P was discretely carried out for every pixel, and they have contributed to contact to the pixel electrode 8. That is, the pixel electrode 8 is connected to pad protection-from-light layer 4P through a contact hole PCN. Pad protection-from-light layer 4P are pulled out through a contact hole JCN, and are connected to electrode 12B. It pulls out to the appearance mentioned above and electrical connection of the electrode 12B is carried out to the drain field D of TFT7 through the contact hole DCN. All fields other than pixel opening are shaded by mask protection-from-light layer 4M and pad protection-from-light layer 4P, and the superposition of the drawer electrodes 12A and 12B to the incidence from an opposite substrate side.

[0006] On the other hand, the protection-from-light layer 5 is formed in the reverse side in the opposite substrate 2 of the pixel transistor section. This is called a "lower layer protection-from-light layer." The source / drain edge of the pixel transistor 7 at least are shaded in this lower layer protection-from-light layer 5. Thus, the LDD fields 71 and 72 are formed in the source / drain edge currently shaded. Generally the lower layer protection-from-light layer 5 is formed from the silicide of a refractory metal. For example, it consists of WSi and has the thickness of 200nm.

[0007]

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[0008] Drawing 6 is the typical top view of the conventional liquid crystal display shown in drawing 5 , and expresses only 1 pixel. The liquid crystal display is equipped with two or more signal wiring 12 and gate wiring which cross mutually so that it may illustrate. The pixel is prepared in the intersection with gate wiring arranged on the signal wiring 12 allotted in the direction of a train (lengthwise direction), and a line writing direction (longitudinal direction). A pixel contains a pixel electrode, the thin film transistor which drives this, and the protection-from-light band (protection-from-light layer) which covers a thin film transistor from outdoor daylight. The thin film transistor makes the semi-conductor thin film 10 the barrier layer, it connected with signal wiring 12 through the contact hole SCN, and, similarly the source field has connected the drain field to a pixel electrode (not shown) through a contact hole DCN. Moreover, the gate electrode G is formed as some gate wiring. In addition, gate wiring is formed with the semi-conductor thin film (2poly) which becomes layer with the another semi-conductor

thin film (1poly) 10. Furthermore, the auxiliary capacity 13 is formed in the pixel. This auxiliary capacity 13 has a laminated structure which pinched gate dielectric film and the dielectric thin film of this layer between the semi-conductor thin film (1poly) 10 and the semi-conductor thin film (2poly) 14. While the semi-conductor thin film 10 used as the bottom electrode of the auxiliary capacity 13 serves as a drain of a thin film transistor, and same electric potential, the semi-conductor thin film 14 used as the top electrode of the auxiliary capacity 13 is connected to the drawer electrode (not shown) which consists of the upper aluminum through a contact hole CCN. This drawer electrode is further connected to the upper mask protection-from-light layer through the contact hole MCN. In addition, the pixel electrode (not shown) is connected to the drain field D of a thin film transistor through contact holes PCN, JCN, and DCN. The gate electrode G is formed with the semi-conductor thin film 14 (2poly), is extended in a longitudinal direction as it is, and forms gate wiring so that it may illustrate. Although this semi-conductor thin film 14 also serves as a top electrode of the auxiliary capacity 13, gate wiring differs from potential. In spite of being formed with the same semi-conductor thin film 14 for this reason, it is necessary to dissociate electrically and gate wiring and the top electrode of the auxiliary capacity 13 need to secure a predetermined gap (GAP) among both. With this pixel structure, since gate wiring and the top electrode of the auxiliary capacity 13 are arranged in parallel mutually, it is necessary to take GAP and, for this reason, a numerical aperture is restricted among both. Although it is easily presumed that it is effective to form gate wiring and the top electrode of the auxiliary capacity 13 in another layer in order to improve a numerical aperture, with structure, it is not the appearance conventionally which is shown in drawing 6 .

[0009] Drawing 7 is a graph which shows the relation of the numerical aperture and auxiliary capacity (Cs) area in structure conventionally which was shown in drawing 6 . If it is going to take a large numerical aperture, since auxiliary capacity area will fall victim, auxiliary capacity area will decrease rapidly with a numerical aperture rise. Gate wiring and the top electrode (auxiliary capacity wiring) of auxiliary capacity are these layers, and this is because parallel arrangement is carried out. With such parallel arrangement structure, an improvement of a numerical aperture and reservation of auxiliary capacity area cannot be incompatible, and have been the technical problem which should be solved.

[0010]

[Means for Solving the Problem] This invention aims at improving the pixel numerical aperture of the thin film semiconductor equipment used as a drive substrate of an active matrix liquid crystal display in view of the technical problem of a Prior art mentioned above. The following means were provided in order to attain the starting purpose. This invention is equipped with two or more signal wiring and gate wiring which cross mutually, and the pixel allotted to each intersection of both wiring on an insulating substrate. Namely, each pixel The protection-from-light band which covers at least a pixel electrode, the thin film transistor which drives this, and this thin film transistor from outdoor daylight is included. In the thin film semiconductor equipment by which the source of this thin film transistor is connected to this signal wiring, a drain is connected to this pixel electrode, and the gate electrode is connected to this gate wiring said protection-from-light band It consists of the first conductive layer and at least a part is used for this gate wiring. Said gate electrode It consists of the second different conductive layer from the first conductive layer, and this first conductive layer used for gate wiring and this second conductive layer that becomes a gate electrode are characterized by connecting electrically mutually within each pixel.

[0011] The second conductive layer which constitutes said gate electrode is preferably divided for every pixel, and the part of each second divided conductive layer is electrically connected with this first conductive layer used for this gate wiring within each pixel. Or the first conductive layer which constitutes said gate wiring is divided for every pixel, and the part of each first divided conductive layer is electrically connected with this second conductive layer that serves as this gate electrode within each pixel. Moreover, said protection-from-light band consists of a conductive layer of the bilayer which covers this thin film transistor from up-and-down [both], and the one of the two is used for this gate wiring as the first conductive layer. Or said protection-from-light band consists of a conductive layer of the monolayer which covers this thin film transistor from up-and-down inner one side, and this is used

for this gate wiring as the first conductive layer. Moreover, each pixel is the second conductive layer and this layer from which one side of the electrode of this vertical pair constitutes this gate electrode including the auxiliary capacity which sandwiched the dielectric with the electrode of a vertical pair, in order to hold the signal charge written in this pixel electrode from signal wiring through this thin film transistor.

[0012] According to this invention, the protection-from-light band which covers a thin film transistor from outdoor daylight consists of the first conductive layer, and is using the part for gate wiring at least. On the other hand, the gate electrode consisted of the second different conductive layer from the first conductive layer, and has connected the protection-from-light band of each other with the gate electrode electrically within each pixel. It becomes unnecessary thus, to form gate wiring and an auxiliary capacity line in this layer by using a protection-from-light layer for gate wiring. For example, if a lower layer protection-from-light layer is used for gate wiring, auxiliary capacity wiring can be formed in a gate electrode and this layer in piles on it. Like the former, since it becomes unnecessary to secure between [GAP] lines between gate wiring of this layer, and auxiliary capacity wiring, it leads to an improvement of the part numerical aperture.

[0013]

[Embodiment of the Invention] With reference to a drawing, the gestalt of operation of this invention is explained to a detail below. Drawing 1 is the typical top view of an example of the liquid crystal display concerning this invention, and has shown especially 1 pixel. Especially drawing 1 expresses the flat-surface configuration of the thin film semiconductor equipment which becomes the drive substrate side of a liquid crystal display. Thin film semiconductor equipment is equipped with two or more signal wiring 12 and gate wiring which cross mutually, and the pixel allotted to each intersection of both wiring on the insulating substrate so that it may illustrate. By a diagram, the pixel of a piece is allotted to the intersection of one signal wiring 12 allotted to the lengthwise direction and gate wiring of one arranged on the longitudinal direction. Each pixel contains at least the pixel electrode (not shown), the thin film transistor which drives this, and the protection-from-light layer (protection-from-light band) 5 which covers a thin film transistor from outdoor daylight. The thin film transistor makes the component field the semi-conductor thin film 10 formed on the protection-from-light layer 5 in a lower layer. The source of a thin film transistor is connected to signal wiring 12 through a contact hole SCN, a drain is connected to a pixel electrode (not shown) through contact holes DCN, JCN, and PCN, and the gate electrode G is connected to gate wiring. In addition, this gate electrode G is formed with another semi-conductor thin film (2poly) 14 which is in the upper layer from the semi-conductor thin film (1poly) 10.

[0014] As a description matter, the protection-from-light layer 5 consists of the first conductive layer, and at least the part is used for gate wiring. The gate electrode G consists of the second different conductive layer (namely, semi-conductor thin film 14 with which the impurity was poured in by high concentration) from the first conductive layer. The first conductive layer used for gate wiring and the second conductive layer (semi-conductor thin film 14) which becomes the gate electrode G are mutually connected electrically through the contact hole GCN within each pixel. That is, in this invention, the gate electrode G and gate wiring are another layers, and it has solid composition which both connect mutually per pixel through a contact hole GCN. Here, the second conductive layer (semi-conductor thin film 14) which constitutes the gate electrode G is divided for every pixel, and the part (gate electrode G) of each second divided conductive layer is electrically connected with the first conductive layer (protection-from-light layer 5) currently used for gate wiring within each pixel.

[0015] In addition to the thin film transistor and pixel electrode which were mentioned above, the pixel is equipped with the auxiliary capacity 13. The auxiliary capacity 13 holds the signal charge written in the pixel electrode from signal wiring 12 through the thin film transistor, maintains drawing grace, and has a laminated structure which sandwiched the dielectric with the electrode of a vertical pair. While the top electrode of the auxiliary capacity 13 is the second conductive layer (semi-conductor thin film 14) and this layer which constitute the gate electrode G, bottom electrodes are the semi-conductor thin film 10 and this layer. Therefore, a dielectric consists of gate dielectric film pinched among the electrodes 14 and 10 of a vertical pair, and an insulator layer of this layer. The auxiliary capacity 13 becomes possible

[forming in piles on the protection-from-light layer 5 which constitutes gate wiring] so that clearly from drawing. Therefore, compared with the former, a pixel numerical aperture is sharply improvable. This is the realized structure by substituting the protection-from-light layer 5 of another layer for some of gate electrodes G and gate wiring which was these layers conventionally. That is, while gate wiring is formed in the lower layer protection-from-light layer 5 which consists of WSi, the gate electrode G is formed with the semi-conductor thin film (2poly) 14 as usual. Both of each other are electrically connected through a contact hole GCN. On the other hand, the top electrode of the auxiliary capacity 13 is formed with the gate electrode G and the semi-conductor thin film (2poly) 14 of this layer. since it is formed with another layer, gate wiring and the top electrode (auxiliary capacity wiring) of the auxiliary capacity 13 become possible [forming the auxiliary capacity 13 on the protection-from-light layer 5 used as gate wiring], can boil a numerical aperture markedly and can improve.

[0016] Drawing 2 shows the cross-section structure of the liquid crystal display cut along with X-X-ray shown in drawing 1 . This liquid crystal display consists of substrates 1 and 2 of a pair each other joined through the predetermined gap, and liquid crystal 3 held in this gap so that it may illustrate. While one substrate 1 has the pixel allotted to each intersection of two or more signal wiring 12 and gate wiring which cross mutually, and both wiring, the substrate (opposite substrate) 2 of another side has the electrode (counterelectrode) 6 which counters each pixel.

[0017] The lower layer protection-from-light layer 5 is formed in the front face of the lower substrate 1, and a thin film transistor and the auxiliary capacity 13 are formed through the insulator layer 9 on it. The thin film transistor has the top gate structure where the gate electrode G was arranged through gate dielectric film 11 on the gate electrode 10 of dual structure. Electrical connection is carried out to the protection-from-light layer 5 which was mentioned above and which serves as gate wiring through a contact hole GCN by dividing the gate electrode G for every pixel like. On the other hand, the auxiliary capacity 13 consists of a lower semi-conductor thin film 10, an upper semi-conductor thin film 14, and gate dielectric film 11 held among both. The top electrode of the auxiliary capacity 13 and the gate electrode G consist of semi-conductor thin films (2poly) 14 of this layer so that clearly from drawing. The thin film transistor and the auxiliary capacity 13 which have the starting configuration are covered with the interlayer insulation film, and the signal wiring 12 mentioned above and drawer electrode 12C are formed on it. Such signal wiring 12 and drawer electrode 12C consist of aluminum, and the front face is covered with the flattening film. On the flattening film, the upper protection-from-light layer 4 is formed. Thus, with this operation gestalt, the protection-from-light band for intercepting outdoor daylight consists of a conductive layer of the bilayer which covers a thin film transistor from up-and-down [both], and that one of the two is used for gate wiring as the first conductive layer. The configuration that replace with this, a protection-from-light band consists of a conductive layer of the monolayer which covers a thin film transistor from up-and-down inner one side, and this is used for gate wiring as the first conductive layer may be used. In this example, the top electrode of the auxiliary capacity 13 is pulled out through a contact hole CCN, and is carrying out electrical connection to electrode 12C. Furthermore, electrical connection of this drawer electrode 12C is carried out to the upper protection-from-light layer 4 through the contact hole MCN. Thereby, fixed potential is impressed to the top electrode of the auxiliary capacity 13. Furthermore, the upper protection-from-light layer 4 is covered by the protective coat, and the pixel electrode (not shown) is formed on it.

[0018] With reference to drawing 2 , the manufacturing method of this liquid crystal display is explained succeedingly. This liquid crystal display consists of substrates 1 and 2 of a pair each other joined through the predetermined gap, and liquid crystal 3 held in this gap. In order to manufacture this, while forming the pixel allotted to each intersection of two or more signal wiring 12 and gate wiring which intersect one substrate 1 mutually, and both wiring, the electrode 6 which counters each pixel is formed in the substrate 2 of another side. The protection-from-light band 5 which covers at least a pixel electrode, the thin film transistor which drives this, and this thin film transistor from outdoor daylight is formed in each pixel. The source of a thin film transistor is connected to signal wiring 12, a drain is connected to a pixel electrode, and the gate electrode G is connected to gate wiring. In that case, the protection-from-light band 5 uses the part for gate wiring at least while forming it by the first conductive

layer. Moreover, the gate electrode G is formed by the second different conductive layer 14 from the first conductive layer. And the first conductive layer used for gate wiring and the second conductive layer 14 which becomes the gate electrode G are mutually connected electrically by the contact hole GCN within each pixel. In this example, a protection-from-light band is formed by the conductive layer of the bilayer which covers a thin film transistor from up-and-down [both], and uses protection-from-light band 5 of one of the two for gate wiring as the first conductive layer. Moreover, in order to hold the signal charge written in a pixel electrode through a thin film transistor from signal wiring 12, the auxiliary capacity 13 which sandwiched the gate dielectric film 11 used as a dielectric with the electrode (10 14) of a vertical pair is formed in each pixel, and it forms so that it may become the second conductive layer 14 and this layer from which one side of the electrode of a vertical pair constitutes the gate electrode G.

[0019] Drawing 3 is the mimetic diagram showing the equal circuit for 1 pixel. (A) shows the circuit of this invention and (B) expresses the example of reference. Although it is the example of reference of (B) first, the lower layer protection-from-light layer 5 does not become some gate wiring, but this is connected to touch-down potential. With the starting configuration, it will be made to a LDD field so that the parasitic transistor by the metal protection-from-light layer 5 may surround by the dotted line. Since the potential of the protection-from-light layer 5 is usually grounded by immobilization, it is committed in the direction which is always going to turn off a parasitic transistor. In order to prevent this, it is impossible to lower the high impurity concentration of a LDD field beyond a fixed limit. However, for drawing grace maintenance, there is a demand of wanting to lower the high impurity concentration of a LDD field from the present condition to about 1/3, with the formation of the large quantity of light in recent years.

[0020] With the configuration of this invention shown in (A) on the other hand, although the parasitic transistor by the metal protection-from-light layer 5 is made like the example of reference, the potential of the protection-from-light layer 5 is always kept equal to gate potential through the contact hole GCN. Therefore, ON/OFF of the parasitic transistor enclosed with a dotted line synchronize with an ontic thin film transistor completely. For this reason, the high impurity concentration of a LDD field can be reduced dramatically, and, as a result, improvement in maintenance of drawing grace can be realized. In addition, the picture signal Vsig supplied to signal wiring 12 is written in a pixel electrode through the drain field D among drawing from the source field S of a thin film transistor TFT. By a diagram, the potential written in the pixel electrode is expressed with Vpxl. On the other hand, the potential impressed to the gate electrode G of a thin film transistor is expressed with Vg.

[0021] Drawing 4 is the mimetic diagram showing the connection relation between the gate electrode G and the protection-from-light layer 5 for which gate wiring is substituted. While (A) expresses typically the connection relation of the operation gestalt shown in drawing 1 and each pixel electrode G is divided per pixel, the protection-from-light layer 5 used as gate wiring is continuing between pixels. Electrical connection of the divided each gate electrode G is carried out to the lower layer protection-from-light layer 5 through the corresponding contact hole GCN. The deformation of a substrate is increasing as a side effect of the multilayering which forms a metal thin film layer and a semi-conductor thin film layer in piles. This has had serious effect on the control in the assembly and the mounting process of a panel. It has become clear that it is the big factor of substrate deformation to form continuously gate wiring which consists of a semi-conductor thin film (2poly) conventionally especially along the longitudinal direction of a panel. On the other hand, in this invention, since the gate electrode G which expressed to (A) typically and which consists of 2poly like is divided for every pixel, reduction-ization of substrate deformation is expectable. Furthermore, since it is not used as wiring like the former, thickness of the gate electrode G itself can be made thin. It is possible to lower substrate deformation also by this.

[0022] (B) is the configuration which also divided the lower layer protection-from-light layer 5 which constitutes gate wiring per pixel in addition to the gate electrode G. It has composition which carries out electrical connection continuously in the contact hole GCN in which the gate electrode G divided, respectively and two lower layer protection-from-light layers 5 per pixel were formed. Since the lower layer protection-from-light layer 5 was also divided, it is possible to make substrate deformation still

smaller.

[0023] While (C) divides the protection-from-light layer 5, it forms the gate electrode G continuously between pixels. Furthermore, in the case of (D), it has connected mutually in the contact hole GCN in which both were prepared for every pixel, holding continuously the gate electrode G and the lower layer protection-from-light layer 5. With such a configuration, since a flow is securable on the other hand even if one side is disconnected among the conductive layers of a vertical bilayer, the merit that failure does not occur as a result is obtained.

[0024]

[Effect of the Invention] According to this invention, an improvement of a numerical aperture is attained like by the thing which were explained above and for which a protection-from-light layer is used for gate wiring. Moreover, double-gate structure whose semi-conductor thin film which serves as a barrier layer of a thin film transistor with the protection-from-light layer which serves as gate wiring, and a gate electrode is pinched from the upper and lower sides can be realized, and it leads to expansion of the design margin of a thin film transistor. For example, reduction-ization is attained in the high impurity concentration of a LDD field by considering as double-gate structure, and a thin film transistor with that much little optical leak is obtained. Furthermore, it is possible to control deformation of a substrate by dividing the protection-from-light layer used as a gate electrode or gate wiring per pixel.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the typical top view of the liquid crystal display concerning this invention.
[Drawing 2] It is the typical sectional view of the liquid crystal display shown in drawing 1 .
[Drawing 3] It is the representative circuit schematic for 1 pixel of the liquid crystal display shown in drawing 1 and drawing 2 .
[Drawing 4] It is the mimetic diagram showing the electric connection relation between the pixel electrode of a liquid crystal display, and a protection-from-light layer concerning this invention.
[Drawing 5] It is the sectional view showing an example of the conventional liquid crystal display.
[Drawing 6] It is the top view showing an example of the conventional liquid crystal display.
[Drawing 7] It is the graph which shows the relation between a pixel numerical aperture and auxiliary capacity area.
[Description of Notations]
5 [... Auxiliary capacity, 14 / ... A semi-conductor thin film, G / ... Gate electrode] ... A protection-from-light layer (gate wiring), 10 ... A semi-conductor thin film, 12 ... Signal wiring, 13

[Translation done.]

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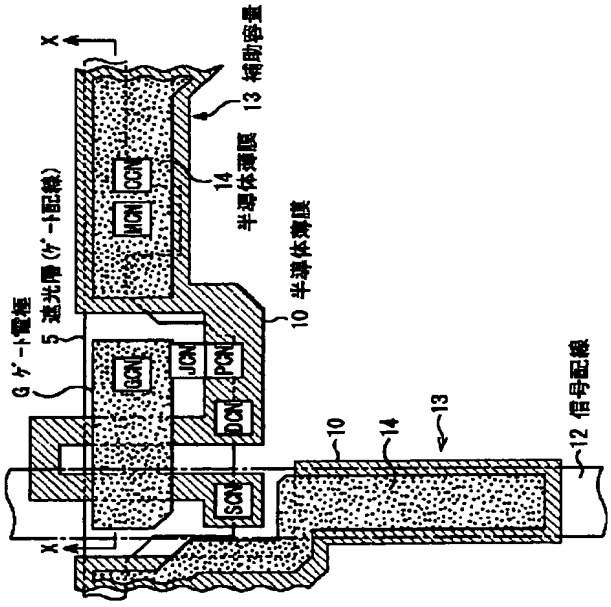
(54)【発明の名称】　薄膜半導体装置及び液晶表示装置とこれらの製造方法

(57)【要約】
【課題】　アクティブマトリクス型液晶表示装置の駆動基板として使われる薄膜半導体装置の画素開口率を改善する。
【解決手段】　薄膜半導体装置は、互いに交差する複数の信号配線１２及びゲート配線と、両配線の各交差部に配された画素とを絶縁性の基板上に備える。各画素は、少なくとも画素電極と、これを駆動する薄膜トランジスタと、薄膜トランジスタを外光から遮蔽する遮光帯５とを含む。薄膜トランジスタのソースは信号配線１２に接続され、ドレインは画素電極に接続され、ゲート電極Ｇはゲート配線に接続されている。遮光帯５は、第一の導電層からなり少なくとも一部がゲート配線に使用される。ゲート電極Ｇは、第一の導電層とは異なる第二の導電層からなる。ゲート配線に使用される第一の導電層と、ゲート電極Ｇになる第二の導電層とが、コンタクトホールＧＣＮを介して各画素内で互いに電気的に接続されている。



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【特許請求の範囲】

【請求項１】　互いに交差する複数の信号配線及びゲート配線と、両配線の各交差部に配された画素とを絶縁性の基板上に備え、

各画素は、少なくとも画素電極と、これを駆動する薄膜トランジスタと、該薄膜トランジスタを外光から遮蔽する遮光帯とを含み、

該薄膜トランジスタのソースは該信号配線に接続され、ドレインは該画素電極に接続され、ゲート電極は該ゲート配線に接続されている薄膜半導体装置において、

前記遮光帯は、第一の導電層からなり少なくとも一部が該ゲート配線に使用され、

前記ゲート電極は、第一の導電層とは異なる第二の導電層からなり、

ゲート配線に使用される該第一の導電層と、ゲート電極になる該第二の導電層とが、各画素内で互いに電気的に接続されていることを特徴とする薄膜半導体装置。

【請求項２】　前記ゲート電極を構成する第二の導電層は各画素毎に分断されており、分断された個々の第二の導電層の部分は各画素内で該ゲート配線に使用される該第一の導電層と電気的に接続されていることを特徴とする請求項１記載の薄膜半導体装置。

【請求項３】　前記ゲート配線を構成する第一の導電層は各画素毎に分断されており、分断された個々の第一の導電層の部分は各画素内で該ゲート電極となる該第二の導電層と電気的に接続されていることを特徴とする請求項１記載の薄膜半導体装置。

【請求項４】　前記遮光帯は、該薄膜トランジスタを上下の両方から遮蔽する二層の導電層からなり、その片方が第一の導電層として該ゲート配線に使用されていることを特徴とする請求項１記載の薄膜半導体装置。

【請求項５】　前記遮光帯は、該薄膜トランジスタを上下の内片側から遮蔽する単層の導電層からなり、これが第一の導電層として該ゲート配線に使用されていることを特徴とする請求項１記載の薄膜半導体装置。

【請求項６】　各画素は、該薄膜トランジスタを介して信号配線から該画素電極に書き込まれた信号電荷を保持するために誘電体を上下一対の電極で挟んだ補助容量を含み、該上下一対の電極の一方が該ゲート電極を構成する第二の導電層と同層であることを特徴とする請求項１記載の薄膜半導体装置。

【請求項７】　所定の間隙を介して互いに接合した一対の基板と、該間隙に保持された液晶とからなり、

一方の基板は、互いに交差する複数の信号配線及びゲート配線と、両配線の各交差部に配された画素を有する一方、他方の基板は各画素に対向する電極を有し、

各画素は、少なくとも画素電極と、これを駆動する薄膜トランジスタと、該薄膜トランジスタを外光から遮蔽する遮光帯とを含み、

該薄膜トランジスタのソースは該信号配線に接続され、

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ドレインは該画素電極に接続され、ゲート電極は該ゲート配線に接続されている液晶表示装置において、

前記遮光帯は、第一の導電層からなり少なくとも一部が該ゲート配線に使用され、

前記ゲート電極は、第一の導電層とは異なる第二の導電層からなり、

ゲート配線に使用される該第一の導電層と、ゲート電極になる該第二の導電層とが、各画素内で互いに電気的に接続されていることを特徴とする液晶表示装置。

【請求項８】　前記ゲート電極を構成する第二の導電層は各画素毎に分断されており、分断された個々の第二の導電層の部分は各画素内で該ゲート配線に使用される該第一の導電層と電気的に接続されていることを特徴とする請求項７記載の液晶表示装置。

【請求項９】　前記ゲート配線を構成する第一の導電層は各画素毎に分断されており、分断された個々の第一の導電層の部分は各画素内で該ゲート電極となる該第二の導電層と電気的に接続されていることを特徴とする請求項７記載の液晶表示装置。

【請求項１０】　前記遮光帯は、該薄膜トランジスタを上下の両方から遮蔽する二層の導電層からなり、その片方が第一の導電層として該ゲート配線に使用されていることを特徴とする請求項７記載の液晶表示装置。

【請求項１１】　前記遮光帯は、該薄膜トランジスタを上下の内片側から遮蔽する単層の導電層からなり、これが第一の導電層として該ゲート配線に使用されていることを特徴とする請求項７記載の液晶表示装置。

【請求項１２】　各画素は、該薄膜トランジスタを介して該信号配線から該画素電極に書き込まれた信号電荷を保持するために誘電体を上下一対の電極で挟んだ補助容量を含み、該上下一対の電極の一方が該ゲート電極を構成する第二の導電層と同層であることを特徴とする請求項７記載の液晶表示装置。

【請求項１３】　互いに交差する複数の信号配線及びゲート配線と、両配線の各交差部に配された画素とを絶縁性の基板上に備え、各画素は、少なくとも画素電極と、これを駆動する薄膜トランジスタと、該薄膜トランジスタを外光から遮蔽する遮光帯とを含み、該薄膜トランジスタのソースは該信号配線に接続され、ドレインは該画素電極に接続され、ゲート電極は該ゲート配線に接続されている薄膜半導体装置の製造方法において、

前記遮光帯は、第一の導電層で形成すると共に少なくともその一部を該ゲート配線に使用し、

前記ゲート電極は、第一の導電層とは異なる第二の導電層で形成し、

ゲート配線に使用する該第一の導電層とゲート電極になる該第二の導電層とを各画素内で互いに電気的に接続することを特徴とする薄膜半導体装置の製造方法。

【請求項１４】　前記ゲート電極を構成する第二の導電層を各画素毎に分断すると共に、分断した個々の第二の

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導電層の部分を各画素内で該ゲート配線に使用する該第一の導電層と電気的に接続することを特徴とする請求項１３記載の薄膜半導体装置の製造方法。

【請求項１５】　前記ゲート配線を構成する第一の導電層を各画素毎に分断すると共に、分断した個々の第一の導電層の部分を各画素内で該ゲート電極となる該第二の導電層と電気的に接続することを特徴とする請求項１３記載の薄膜半導体装置の製造方法。

【請求項１６】　前記遮光帯は、該薄膜トランジスタを上下の両方から遮蔽する二層の導電層で形成し、その片方を第一の導電層として該ゲート配線に使用することを特徴とする請求項１３記載の薄膜半導体装置の製造方法。

【請求項１７】　前記遮光帯は、該薄膜トランジスタを上下の内片側から遮蔽する単層の導電層で形成し、これを第一の導電層として該ゲート配線に使用することを特徴とする請求項１３記載の薄膜半導体装置の製造方法。

【請求項１８】　該信号配線から該薄膜トランジスタを介して該画素電極に書き込まれる信号電荷を保持するために誘電体を上下一対の電極で挟んだ補助容量を各画素に形成し、該上下一対の電極の一方が該ゲート電極を構成する第二の導電層と同層になる様に形成することを特徴とする請求項１３記載の薄膜半導体装置の製造方法。

【請求項１９】　所定の間隙を介して互いに接合した一対の基板と、該間隙に保持された液晶とからなり、一方の基板には互いに交差する複数の信号配線及びゲート配線と両配線の各交差部に配された画素を形成する一方、他方の基板には各画素に対向する電極を形成し、各画素には、少なくとも画素電極と、これを駆動する薄膜トランジスタと、該薄膜トランジスタを外光から遮蔽する遮光帯とを形成し、該薄膜トランジスタのソースを該信号配線に接続し、ドレインを該画素電極に接続し、ゲート電極を該ゲート配線に接続する液晶表示装置の製造方法において、

前記遮光帯は、第一の導電層で形成すると共に少なくともその一部を該ゲート配線に使用し、

前記ゲート電極は、第一の導電層とは異なる第二の導電層で形成し、

ゲート配線に使用する該第一の導電層とゲート電極になる該第二の導電層とを各画素内で互いに電気的に接続することを特徴とする液晶表示装置の製造方法。

【請求項２０】　前記ゲート電極を構成する第二の導電層を各画素毎に分断すると共に、分断した個々の第二の導電層の部分を各画素内で該ゲート配線に使用する該第一の導電層と電気的に接続することを特徴とする請求項１９記載の液晶表示装置の製造方法。

【請求項２１】　前記ゲート配線を構成する第一の導電層を各画素毎に分断すると共に、分断した個々の第一の導電層の部分を各画素内で該ゲート電極となる該第二の導電層と電気的に接続することを特徴とする請求項１９

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記載の液晶表示装置の製造方法。

【請求項２２】　前記遮光帯は、該薄膜トランジスタを上下の両方から遮蔽する二層の導電層で形成し、その片方を第一の導電層として該ゲート配線に使用することを特徴とする請求項１９記載の液晶表示装置の製造方法。

【請求項２３】　前記遮光帯は、該薄膜トランジスタを上下の内片側から遮蔽する単層の導電層で形成し、これを第一の導電層として該ゲート配線に使用することを特徴とする請求項１９記載の液晶表示装置の製造方法。

【請求項２４】　該信号配線から該薄膜トランジスタを介して該画素電極に書き込まれる信号電荷を保持するために誘電体を上下一対の電極で挟んだ補助容量を各画素に形成し、該上下一対の電極の一方が該ゲート電極を構成する第二の導電層と同層になる様に形成することを特徴とする請求項１９記載の液晶表示装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、薄膜半導体装置及び液晶表示装置とこれらの製造方法に関する。より詳しくは、薄膜半導体装置に集積形成される薄膜トランジスタのゲート配線構造及び遮光構造に関する。

【０００２】

【従来の技術】薄膜トランジスタや画素電極を集積形成した薄膜半導体装置は、液晶表示装置の駆動基板に多用されている。特に、プロジェクタ用の液晶表示装置に組み込まれる薄膜半導体装置は、薄膜トランジスタをプロジェクタの強い光源光から遮蔽する為に遮光構造が必須となっており、図５にその一例を示す。図示する様に、液晶表示装置は画素電極８を駆動する為に薄膜トランジスタを用いている。この薄膜トランジスタは、例えば高温ポリシリコンＴＦＴであるが、これに代えて低温ポリシリコンＴＦＴや非晶質シリコンＴＦＴを用いることも可能である。図示の液晶表示装置は、例えば特開平２０００－１３１７１６号公報に開示されている。図示する様に、本液晶表示装置は、画素トランジスタであるＴＦＴ７を有する基板１（ＴＦＴを担持する石英からなる）と、対向基板２とを備え、基板１と対向基板２との間には液晶３が保持される。対向基板２は対向電極６を備えている。

【０００３】基板１は、上層部に画素電極８を有し、下層部にＴＦＴ（薄膜トランジスタ、ここではトップゲート構造のＴＦＴ）７を有する。ＴＦＴ７は、画素電極８を駆動するスイッチング素子としての役割を果たす。ＴＦＴ７は、例えば多結晶シリコンからなる半導体薄膜１０を活性層としている。この半導体薄膜１０は、第一層ポリシリコン（１ｐｏｌｙ）で構成される。半導体薄膜１０の上には、SiO_2 などからなるゲート絶縁膜１１を介して、ゲート電極Ｇが形成されている。このゲート電極Ｇは、第二層ポリシリコン（２ｐｏｌｙ）で構成される。ＴＦＴ７は、ゲート電極Ｇの両側にソース領域Ｓ

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及びドレイン領域Dを有する。ソース／ドレイン端部にＬＤＤ領域が形成されている。ソース領域Ｓ及びドレイン領域Dには、各々引き出し電極１２Ａ，１２Ｂが接続している。各引き出し電極１２Ａ，１２Ｂは、アルミニウムなどのアルミニウム系材料で形成できる。引き出し電極１２ＡはコンタクトホールＳＣＮを介してＴＦＴ７のソース領域Ｓに電気接続し、他方の引き出し電極１２Ｂは同じくコンタクトホールＤＣＮを介してＴＦＴ７のドレイン領域Dに電気接続している。

【０００４】半導体薄膜１０には、補助容量１３（Ｃｓ）が形成されている。この補助容量１３（Ｃｓ）は、半導体薄膜１０即ちＴＦＴ７を構成する第一層ポリシリコン（１ｐｏｌｙ）と、半導体薄膜１４即ちゲート電極Ｇを構成する第二層ポリシリコン（２ｐｏｌｙ）とで、ゲート絶縁膜１１を構成するSiO_2などの誘電体膜を挟んだものである。

【０００５】画素電極８を有する上層部と、ＴＦＴ７が形成されている下層部との間の中層部には、遮光層４Ｍ，４Ｐが形成されている。これは、ＴＦＴ７に対して対向基板２側、即ち入射側にある遮光層であり、「上層遮光層」と呼ばれる。上層遮光層は、マスク遮光層４Ｍ及びパッド遮光層４Ｐとからなる。対向基板２側からの入射光に対しては二つの上層遮光層（マスク遮光層４Ｍ及びパッド遮光層４Ｐ）と引き出し電極１２Ａ及び１２Ｂ（ここではアルミニウムにより形成）の重ね合わせにより、画素開口以外の領域全ての遮光を成している。マスク遮光層４Ｍ及びパッド遮光層４Ｐは、共に導電性を有する材料、例えばＴｉなどの金属膜からなる。マスク遮光層４Ｍは画素の行方向（横方向）に沿って連続的にパタニングされており、少なくとも部分的にＴＦＴを遮光する。パッド遮光層４Ｐは画素毎に離散的にパタニングされ、画素電極８とのコンタクトに寄与している。即ち、画素電極８はコンタクトホールＰＣＮを介してパッド遮光層４Ｐに接続する。パッド遮光層４ＰはコンタクトホールＪＣＮを介して引き出し電極１２Ｂに接続する。前述した様に引き出し電極１２ＢはコンタクトホールＤＣＮを介してＴＦＴ７のドレイン領域Dに電気接続している。マスク遮光層４Ｍ及びパッド遮光層４Ｐと、引き出し電極１２Ａ及び１２Ｂの重ね合わせにより、画素開口以外の領域の全てが対向基板側からの入射に対して遮光される。

【０００６】一方、画素トランジスタ部の対向基板２とは逆の側に、遮光層５が形成されている。これを「下層遮光層」と称する。少なくとも画素トランジスタ７のソース／ドレイン端部は、この下層遮光層５で遮光されている。この様に遮光されているソース／ドレイン端部に、ＬＤＤ領域７１，７２が形成されているのである。下層遮光層５は、一般に高融点金属のシリサイドから形成される。例えば、ＷＳｉからなり２００ｎｍの厚みを有する。

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【０００７】

【発明が解決しようとする課題】近年加速する液晶プロジェクタの高輝度化に対応して、図５に示した様な液晶パネルの透過率向上が要求されている。合わせて、プロジェクタ用光源から発する大光量下における画像品位の維持が要求されている。従来、その為の手法として、（１）画素開口率向上による透過率改善と（２）補助容量（Ｃｓ面積）増による画像品位の維持が実施されており、市場の要求に答えてきた。しかしながら、手法（１）と（２）は本質的に相反している。即ち、Ｃｓ面積の増大はそのまま開口率の低下に直結する。従来、（１）と（２）の手法を平行して進めることができたのは、画素レイアウト上余裕があったからである。しかし、液晶プロジェクタの高精細化が進むに連れ、レイアウト上の余裕はなくなってきており、一層の高開口率化を達成する為には、従来の画素構造の延長線上では最早不可能になっている。

【０００８】図６は、図５に示した従来の液晶表示装置の模式的な平面図であり、一画素分のみを表わしている。図示する様に、液晶表示装置は、互いに交差する複数の信号配線１２及びゲート配線を備えている。列方向（縦方向）に配された信号配線１２と行方向（横方向）に配されたゲート配線との交差部に、画素が設けられている。画素は、画素電極と、これを駆動する薄膜トランジスタと、薄膜トランジスタを外光から遮蔽する遮光帯（遮光層）とを含む。薄膜トランジスタは半導体薄膜１０を活性層としており、そのソース領域はコンタクトホールＳＣＮを介して信号配線１２に接続し、ドレイン領域は同じくコンタクトホールＤＣＮを介して画素電極（図示せず）に接続している。又、ゲート電極Ｇはゲート配線の一部として形成されている。尚、ゲート配線は半導体薄膜（１ｐｏｌｙ）１０とは別の層になる半導体薄膜（２ｐｏｌｙ）で形成されている。更に、画素には補助容量１３が形成されている。この補助容量１３は、半導体薄膜（１ｐｏｌｙ）１０と、半導体薄膜（２ｐｏｌｙ）１４との間にゲート絶縁膜と同層の誘電体薄膜を挟持した積層構造となっている。補助容量１３の下側電極となる半導体薄膜１０は薄膜トランジスタのドレインと同電位となる一方、補助容量１３の上側電極となる半導体薄膜１４は、コンタクトホールＣＣＮを介して上層のアルミニウムからなる引き出し電極（図示せず）に接続されている。この引き出し電極は更にコンタクトホールＭＣＮを介して上層のマスク遮光層に接続されている。尚、画素電極（図示せず）はコンタクトホールＰＣＮ，ＪＣＮ及びＤＣＮを介して薄膜トランジスタのドレイン領域Dに接続している。図示する様に、ゲート電極Ｇは半導体薄膜１４（２ｐｏｌｙ）で形成されており、そのまま横方向に延長されてゲート配線を形成する。この半導体薄膜１４は補助容量１３の上側電極ともなるが、ゲート配線と電位は異なる。この為、同じ半導体薄

膜１４で形成されているにも関わらず、ゲート配線と補助容量１３の上側電極は電気的に分離する必要があり、両者の間に所定の間隙（ＧＡＰ）を確保する必要がある。この画素構造では、ゲート配線と補助容量１３の上側電極とを互いに平行に配置している為、両者の間にＧＡＰを取る必要があり、この為開口率が制限される。開口率を改善する為には、ゲート配線と補助容量１３の上側電極とを別層にて形成することが有効であることが容易に推定されるが、図６に示す従来構造ではその様になっていない。

【０００９】図７は、図６に示した従来構造における開口率と補助容量（Ｃｓ）面積との関係を示すグラフである。開口率を大きく取ろうとすると、補助容量面積が犠牲となる為、開口率アップと共に補助容量面積が急激に減少してしまう。これは、ゲート配線と補助容量の上側電極（補助容量配線）が同層で且つ平行配置されている為である。この様な平行配置構造では、開口率の改善と補助容量面積の確保は両立し得ず、解決すべき課題となっている。

【００１０】

【課題を解決するための手段】上述した従来の技術の課題に鑑み、本発明はアクティブマトリクス型液晶表示装置の駆動基板として使われる薄膜半導体装置の画素開口率を改善することを目的とする。係る目的を達成する為に以下の手段を講じた。即ち、本発明は、互いに交差する複数の信号配線及びゲート配線と、両配線の各交差部に配された画素とを絶縁性の基板上に備え、各画素は、少なくとも画素電極と、これを駆動する薄膜トランジスタと、該薄膜トランジスタを外光から遮蔽する遮光帯とを含み、該薄膜トランジスタのソースは該信号配線に接続され、ドレインは該画素電極に接続され、ゲート電極は該ゲート配線に接続されている薄膜半導体装置において、前記遮光帯は、第一の導電層からなり少なくとも一部が該ゲート配線に使用され、前記ゲート電極は、第一の導電層とは異なる第二の導電層からなり、ゲート配線に使用される該第一の導電層と、ゲート電極になる該第二の導電層とが、各画素内で互いに電気的に接続されていることを特徴とする。

【００１１】好ましくは、前記ゲート電極を構成する第二の導電層は各画素毎に分断されており、分断された個々の第二の導電層の部分は各画素内で該ゲート配線に使用される該第一の導電層と電気的に接続されている。或いは、前記ゲート配線を構成する第一の導電層は各画素毎に分断されており、分断された個々の第一の導電層の部分は各画素内で該ゲート電極となる該第二の導電層と電気的に接続されている。又、前記遮光帯は、該薄膜トランジスタを上下の両方から遮蔽する二層の導電層からなり、その片方が第一の導電層として該ゲート配線に使用されている。或いは、前記遮光帯は、該薄膜トランジスタを上下の内片側から遮蔽する単層の導電層からなり、これが第一の導電層として該ゲート配線に使用されている。又、各画素は、該薄膜トランジスタを介して信号配線から該画素電極に書き込まれた信号電荷を保持するために誘電体を上下一対の電極で挟んだ補助容量を含み、該上下一対の電極の一方が該ゲート電極を構成する第二の導電層と同層である。

【００１２】本発明によれば、薄膜トランジスタを外光から遮蔽する遮光帯が第一の導電層からなり、少なくともその一部をゲート配線に使用している。一方、ゲート電極は第一の導電層とは異なる第二の導電層からなり、ゲート電極と遮光帯を各画素内で互いに電気的に接続している。この様に、遮光層をゲート配線に利用することで、ゲート配線と補助容量線を同層で形成する必要がなくなる。例えば、下層遮光層をゲート配線に使用すれば、その上に重ねてゲート電極と同層で補助容量配線を形成できる。従来の様に、同層のゲート配線と補助容量配線の間に線間ＧＡＰを確保する必要がなくなるので、その分開口率の改善につながる。

【００１３】

【発明の実施の形態】以下図面を参照して本発明の実施の形態を詳細に説明する。図１は、本発明に係る液晶表示装置の一例の模式的な平面図であり、特に一画素分を示してある。図１は、特に液晶表示装置の駆動基板側となる薄膜半導体装置の平面構成を表わしている。図示する様に、薄膜半導体装置は、互いに交差する複数の信号配線１２及びゲート配線と、両配線の各交差部に配された画素とを絶縁性の基板の上に備えている。図では、縦方向に配した一本の信号配線１２と、横方向に配した一本のゲート配線との交差部に、一個の画素が配されている。各画素は、少なくとも画素電極（図示せず）と、これを駆動する薄膜トランジスタと、薄膜トランジスタを外光から遮蔽する遮光層（遮光帯）５とを含んでいる。薄膜トランジスタは、下層にある遮光層５の上に形成された半導体薄膜１０を素子領域としている。薄膜トランジスタのソースはコンタクトホールＳＣＮを介して信号配線１２に接続され、ドレインはコンタクトホールＤＣＮ、ＪＣＮ及びＰＣＮを介して画素電極（図示せず）に接続され、ゲート電極Ｇはゲート配線に接続されている。尚、このゲート電極Ｇは半導体薄膜（１ｐｏｌｙ）１０より上層にある別の半導体薄膜（２ｐｏｌｙ）１４で形成されている。

【００１４】特徴事項として、遮光層５は第一の導電層からなり少なくとも一部がゲート配線に使用されている。ゲート電極Ｇは、第一の導電層とは異なる第二の導電層（即ち、不純物が高濃度で注入された半導体薄膜１４）からなる。ゲート配線に使用される第一の導電層と、ゲート電極Ｇになる第二の導電層（半導体薄膜１４）とが、各画素内でコンタクトホールＧＣＮを介し互いに電気的に接続されている。即ち、本発明では、ゲート電極Ｇとゲート配線が別層であり、両者がコンタクト

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ホールＧＣＮを介して画素単位で互いに接続する立体構成となっている。ここで、ゲート電極Ｇを構成する第二の導電層（半導体薄膜１４）は、各画素毎に分断されており、分断された個々の第二の導電層の部分（ゲート電極Ｇ）は、各画素内でゲート配線に使用されている第一の導電層（遮光層５）と電気的に接続されている。

【００１５】画素は、上述した薄膜トランジスタ及び画素電極に加え、補助容量１３を備えている。補助容量１３は、薄膜トランジスタを介して信号配線１２から画素電極に書き込まれた信号電荷を保持して、画品位を維持するものであり、誘電体を上下一対の電極で挟んだ積層構造となっている。補助容量１３の上側電極は、ゲート電極Ｇを構成する第二の導電層（半導体薄膜１４）と同層である一方、下側電極は半導体薄膜１０と同層である。従って、誘電体は上下一対の電極１４，１０の間に挟持されたゲート絶縁膜と同層の絶縁膜からなる。図から明らかな様に、補助容量１３はゲート配線を構成する遮光層５の上に重ねて形成することが可能となる。従って、従来に比べ画素開口率を大幅に改善可能である。これは、従来、ゲート電極Ｇと同層であったゲート配線の一部を、別層の遮光層５で代用することにより、実現された構造である。即ち、ゲート配線は例えばＷＳｉからなる下層遮光層５で形成される一方、ゲート電極Ｇは従来と同様に半導体薄膜（２ｐｏｌｙ）１４にて形成される。両者は、コンタクトホールＧＣＮを介して互いに電気的に接続される。一方、補助容量１３の上側電極は、ゲート電極Ｇと同層の半導体薄膜（２ｐｏｌｙ）１４にて形成される。ゲート配線と補助容量１３の上側電極（補助容量配線）とは、別レイヤーにて形成されるので、ゲート配線となる遮光層５の上に補助容量１３を形成することが可能となり、開口率を格段に向上することができる。

【００１６】図２は、図１に示したＸ－Ｘ線に沿って切断した液晶表示装置の断面構造を示している。図示する様に、本液晶表示装置は、所定の間隙を介して互いに接合した一対の基板１，２と、この間隙に保持された液晶３とからなる。一方の基板１は、互いに交差する複数の信号配線１２及びゲート配線と、両配線の各交差部に配された画素を有する一方、他方の基板（対向基板）２は、各画素に対向する電極（対向電極）６を有している。

【００１７】下側の基板１の表面には下層遮光層５が形成されており、その上に絶縁膜９を介して薄膜トランジスタと補助容量１３が形成されている。薄膜トランジスタはデュアル構造のゲート電極１０の上に、ゲート絶縁膜１１を介してゲート電極Ｇを配したトップゲート構造となっている。前述した様に、ゲート電極Ｇは各画素毎に分断されており、コンタクトホールＧＣＮを介して、ゲート配線を兼ねる遮光層５に電気接続している。一方、補助容量１３は、下側の半導体薄膜１０と、上側の

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半導体薄膜１４と、両者の間に保持されたゲート絶縁膜１１とで構成されている。図から明らかな様に、補助容量１３の上側電極とゲート電極Ｇとは、同層の半導体薄膜（２ｐｏｌｙ）１４で構成されている。係る構成を有する薄膜トランジスタ及び補助容量１３は、層間絶縁膜により被覆されており、その上には前述した信号配線１２や引き出し電極１２Ｃが形成されている。これらの信号配線１２及び引き出し電極１２Ｃはアルミニウムからなり、その表面は平坦化膜で被覆されている。平坦化膜の上には、上層遮光層４が形成されている。この様に、本実施形態では外光を遮断する為の遮光帯は、薄膜トランジスタを上下の両方から遮蔽する二層の導電層からなり、その片方が第一の導電層としてゲート配線に使用されている。これに代えて、遮光帯は薄膜トランジスタを上下の内片側から遮蔽する単層の導電層からなり、これが第一の導電層としてゲート配線に使用される構成でもよい。本例では、補助容量１３の上側電極はコンタクトホールＣＣＮを介して引き出し電極１２Ｃに電気接続している。更にこの引き出し電極１２Ｃはコンタクトホールｍｃｎを介して上層遮光層４に電気接続している。これにより、補助容量１３の上側電極には一定の電位が印加される。更に上層遮光層４は保護膜で覆われており、その上に画素電極（図示せず）が形成されている。

【００１８】引き続き図２を参照して本液晶表示装置の製造法を説明する。本液晶表示装置は、所定の間隙を介して互いに接合した一対の基板１，２と、この間隙に保持された液晶３とからなる。これを製造する為に、一方の基板１には互いに交差する複数の信号配線１２及びゲート配線と両配線の各交差部に配された画素を形成する一方、他方の基板２には各画素に対向する電極６を形成する。各画素には、少なくとも画素電極と、これを駆動する薄膜トランジスタと、該薄膜トランジスタを外光から遮蔽する遮光帯５とを形成する。薄膜トランジスタのソースを信号配線１２に接続し、ドレインを画素電極に接続し、ゲート電極Ｇをゲート配線に接続する。その際、遮光帯５は、第一の導電層で形成すると共に少なくともその一部をゲート配線に使用する。又、ゲート電極Ｇは、第一の導電層とは異なる第二の導電層１４で形成する。そして、ゲート配線に使用する第一の導電層とゲート電極Ｇになる第二の導電層１４とを各画素内でコンタクトホールＧＣＮにより互いに電気的に接続する。本例では、遮光帯は、薄膜トランジスタを上下の両方から遮蔽する二層の導電層で形成し、片方の遮光帯５を第一の導電層としてゲート配線に使用する。又、信号配線１２から薄膜トランジスタを介して画素電極に書き込まれる信号電荷を保持するために、誘電体となるゲート絶縁膜１１を上下一対の電極（１０，１４）で挟んだ補助容量１３を各画素に形成し、上下一対の電極の一方がゲート電極Ｇを構成する第二の導電層１４と同層になる様に形成する。

【００１９】図３は、一画素分の等価回路を示す模式図である。（Ａ）は本発明の回路を示し、（Ｂ）は参考例を表わしている。まず（Ｂ）の参考例であるが、これは下層遮光層５がゲート配線の一部となっておらず、接地電位に接続されている。係る構成では、金属遮光層５による寄生トランジスタが点線で囲む様にＬＤＤ領域にできてしまう。遮光層５の電位は固定で通常接地されている為、寄生トランジスタを常にオフしようとする方向に働く。これを防ぐ為に、ＬＤＤ領域の不純物濃度を一定限度以上下げることが不可能である。しかし近年の大光量化に伴い、画品位維持の為にはＬＤＤ領域の不純物濃度を現状より１／３程度まで下げたいという要求がある。

【００２０】一方（Ａ）に示した本発明の構成では、参考例と同様に金属遮光層５による寄生トランジスタはできるものの、遮光層５の電位は常にコンタクトホールＧＣＮを介してゲート電位と等しく保たれている。従って、点線で囲った寄生トランジスタのオン／オフは、実体的な薄膜トランジスタと完全に同期する。この為、ＬＤＤ領域の不純物濃度を劇的に低減可能であり、その結果画品位の維持向上が実現できる。尚、図中、信号配線１２に供給された画像信号Ｖｓｉｇは薄膜トランジスタＴＦＴのソース領域Ｓからドレイン領域Ｄを介して画素電極に書き込まれる。図では、画素電極に書き込まれた電位をＶｐｘｌで表わしてある。一方、薄膜トランジスタのゲート電極Ｇに印加される電位をＶｇで表わしてある。

【００２１】図４は、ゲート電極Ｇと、ゲート配線に代用される遮光層５との接続関係を示す模式図である。（Ａ）は、図１に示した実施形態の接続関係を模式的に表わしたものであり、各画素電極Ｇが画素単位で分断されている一方、ゲート配線となる遮光層５は画素間で連続している。各分断されたゲート電極Ｇは、対応するコンタクトホールＧＣＮを介して下層遮光層５に電気接続されている。金属薄膜層や半導体薄膜層を重ねて形成する多層化の副作用として、基板の変形量が増大しつつある。これは、パネルの組立や実装工程における制御に深刻な影響を与えている。特に、従来半導体薄膜（２ｐｏｌｙ）からなるゲート配線をパネルの横方向に沿って連続的に形成していることが、基板変形の大きな要因であることが判明している。これに対し、本発明では（Ａ）に模式的に表わした様に、２ｐｏｌｙからなるゲート電極Ｇを画素毎に分断している為、基板変形量の低減化が期待できる。更には、従来の様に配線として使用しないのでゲート電極Ｇ自体の膜厚を薄くできる。これによっても、基板変形量を下げることが可能である。

【００２２】（Ｂ）は、ゲート電極Ｇに加え、ゲート配線を構成する下層遮光層５も画素単位で分断した構成である。それぞれ分断されたゲート電極Ｇ及び下層遮光層５を一画素当たり二個設けたコンタクトホールＧＣＮで連続的に電気接続していく構成となっている。下層遮光層５も分断したので、基板変形量を更に小さくすることが可能である。

【００２３】（Ｃ）は、遮光層５を分断する一方、ゲート電極Ｇは画素間で連続的に形成している。更に（Ｄ）の場合は、ゲート電極Ｇ及び下層遮光層５を連続的に保持したまま、両者を画素毎に設けたコンタクトホールＧＣＮで互いに接続している。この様な構成では、上下二層の導電層の内一方が断線しても、他方で導通を確保できる為、結果的に故障が発生しないというメリットが得られる。

【００２４】

【発明の効果】以上説明した様に、本発明によれば、遮光層をゲート配線に利用することで、開口率の改善が可能になる。又、ゲート配線を兼ねる遮光層とゲート電極とで薄膜トランジスタの活性層となる半導体薄膜を上下から挟むダブルゲート構造が実現でき、薄膜トランジスタの設計マージンの拡大につながる。例えば、ダブルゲート構造とすることでＬＤＤ領域の不純物濃度を低減化可能となり、その分光リークの少ない薄膜トランジスタが得られる。更に、ゲート電極もしくはゲート配線として使われる遮光層を画素単位で分断することにより、基板の変形を抑制することが可能である。

【図面の簡単な説明】

【図１】本発明に係る液晶表示装置の模式的な平面図である。

【図２】図１に示した液晶表示装置の模式的な断面図である。

【図３】図１及び図２に示した液晶表示装置の一画素分の等価回路図である。

【図４】本発明に係る液晶表示装置の画素電極と遮光層の電気的な接続関係を示す模式図である。

【図５】従来の液晶表示装置の一例を示す断面図である。

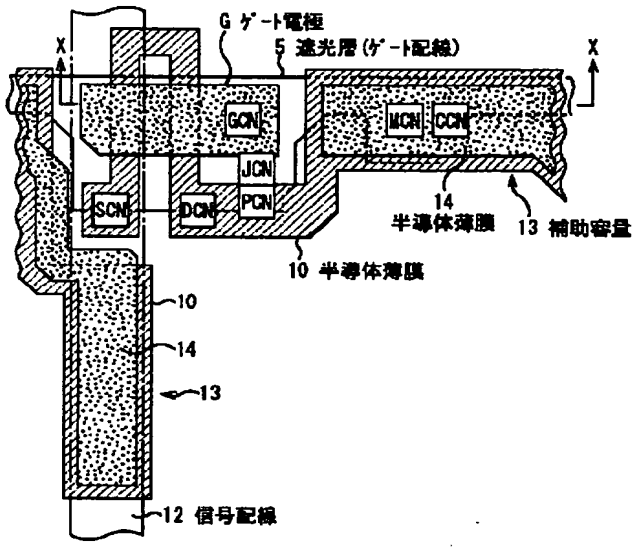
【図６】従来の液晶表示装置の一例を示す平面図である。

【図７】画素開口率と補助容量面積との関係を示すグラフである。

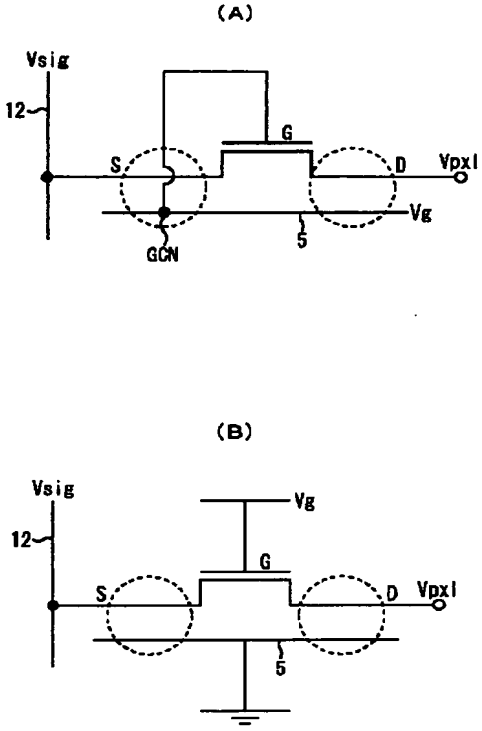
【符号の説明】

５・・・遮光層（ゲート配線）、１０・・・半導体薄膜、１２・・・信号配線、１３・・・補助容量、１４・・・半導体薄膜、Ｇ・・・ゲート電極

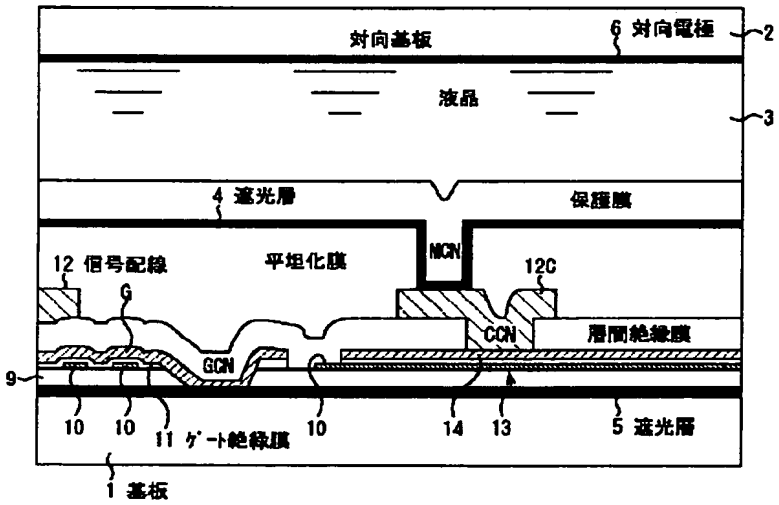
【図１】


G ゲート電極
5 遮光層(ゲート配線)
X
X
GCN
JCN
SCN
DCN
PCN
MCN
CCN
14
半導体薄膜
13 補助容量
10 半導体薄膜
10
14
13
12 信号配線

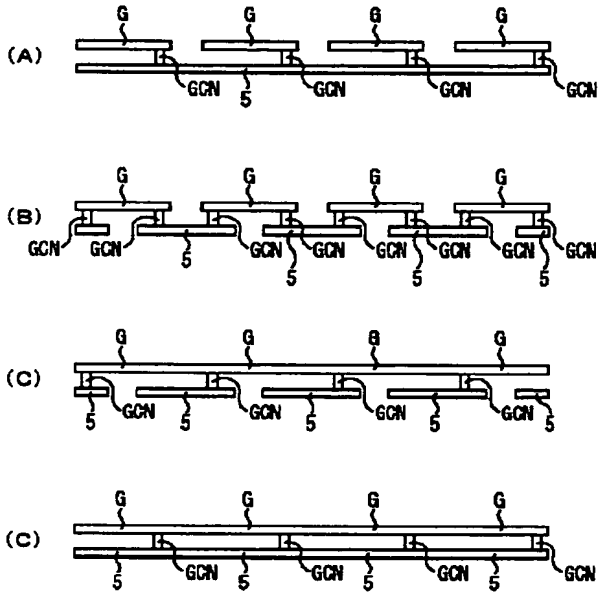
【図３】


(A)
Vsig
12
G
S
D
Vpxl
Vg
GCN
5
(B)
Vsig
Vg
12
G
S
D
Vpxl
5

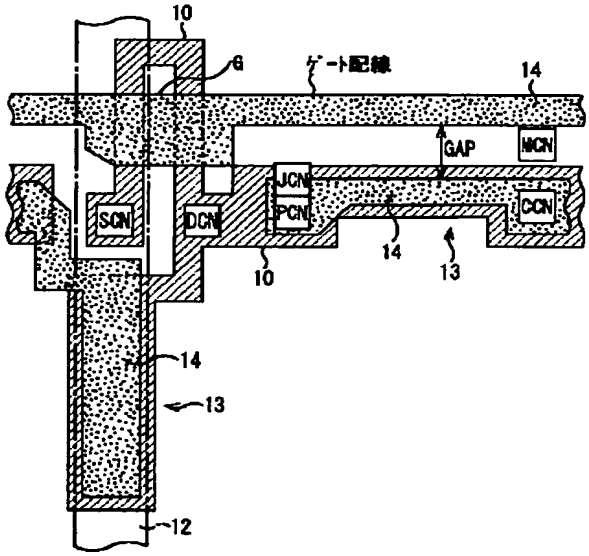
【図２】


対向基板
6 対向電極
2
液晶
3
4 遮光層
保護膜
12 信号配線
平坦化膜
MCN
12C
G
CCN
層間絶縁膜
GCN
9
10
10
11 ゲート絶縁膜
10
14
13
5 遮光層
1 基板

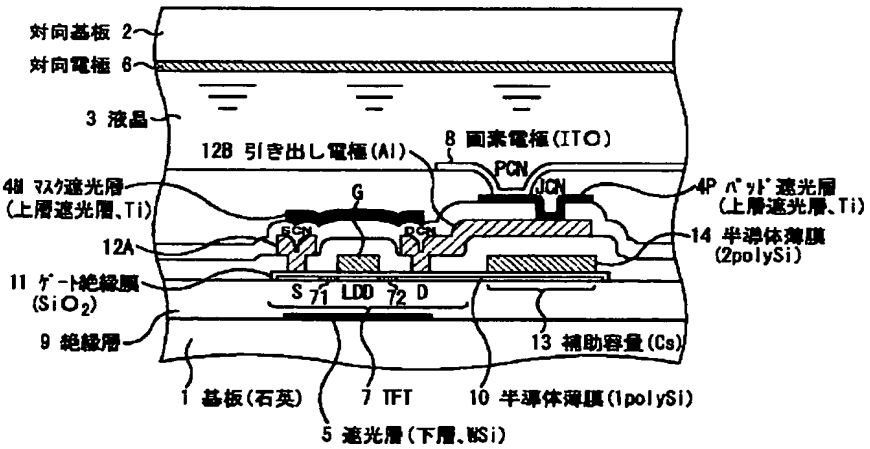
【図４】


(A)
(B)
(C)
(C)
G
GCN
5

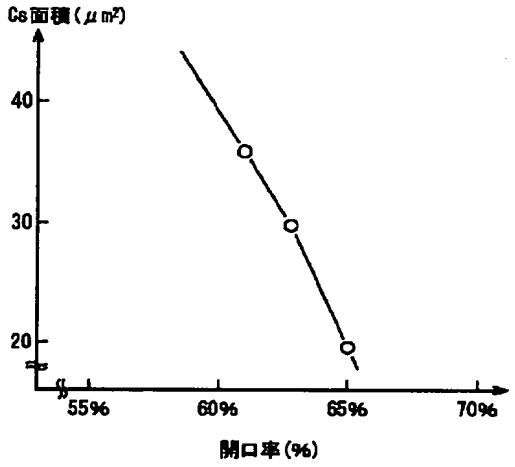
【図６】


10
G
ゲート配線
14
GAP
MCN
JCN
SCN
DCN
PCN
CCN
13
12

【図５】


対向基板 2
対向電極 6
3 液晶
12B 引き出し電極(Al)
8 画素電極(ITO)
4B マスク遮光層
(上層遮光層、Ti)
G
PCN
JCN
4P パッド遮光層
(上層遮光層、Ti)
12A
14 半導体薄膜
(2polySi)
11 ゲート絶縁膜
(SiO2)
S 71 LDD 72 D
9 絶縁層
13 補助容量(Cs)
1 基板(石英)
7 TFT
10 半導体薄膜(1polySi)
5 遮光層(下層、WSi)

【図7】



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